

FIG. 1

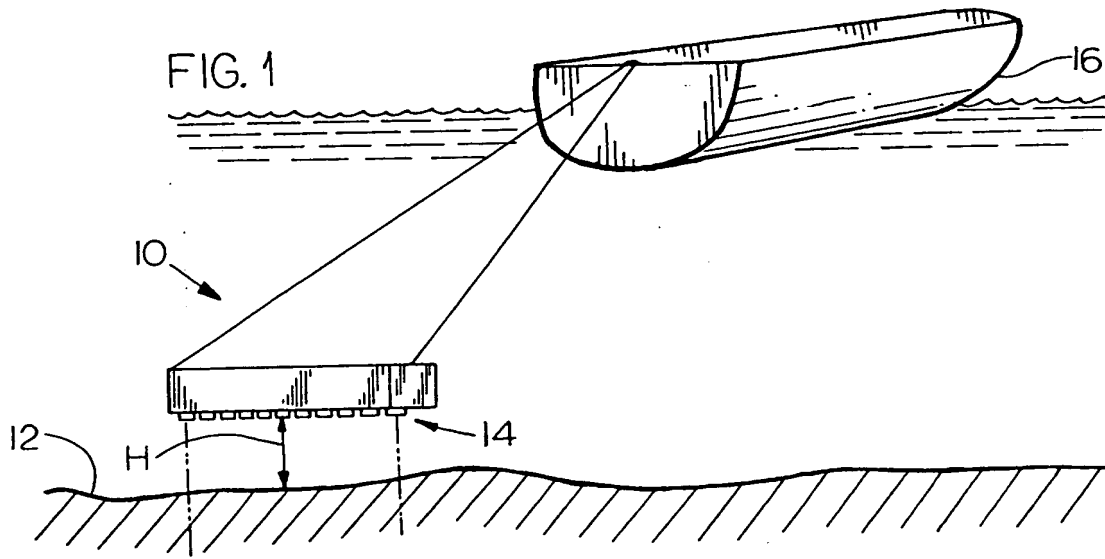


FIG. 2

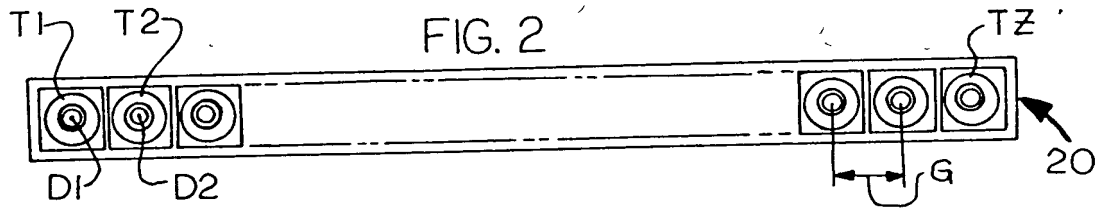
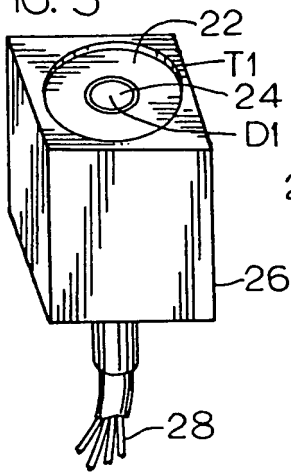
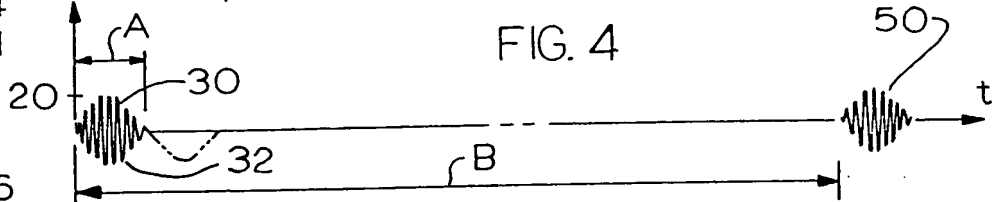


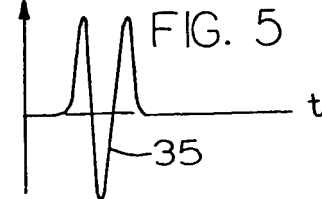
FIG. 3



AMPLITUDE
WATTS/CM.²



AMPL.



AMPL.

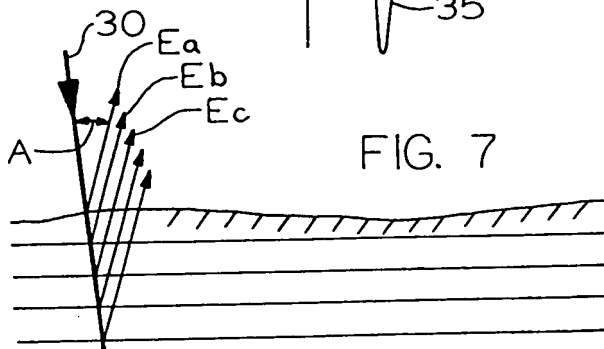
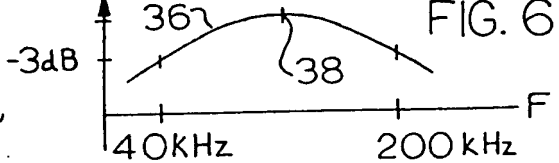


FIG. 7

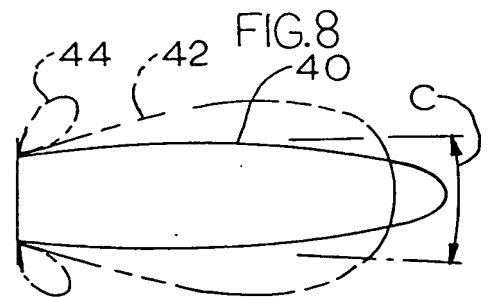


FIG. 8

FIG. 9

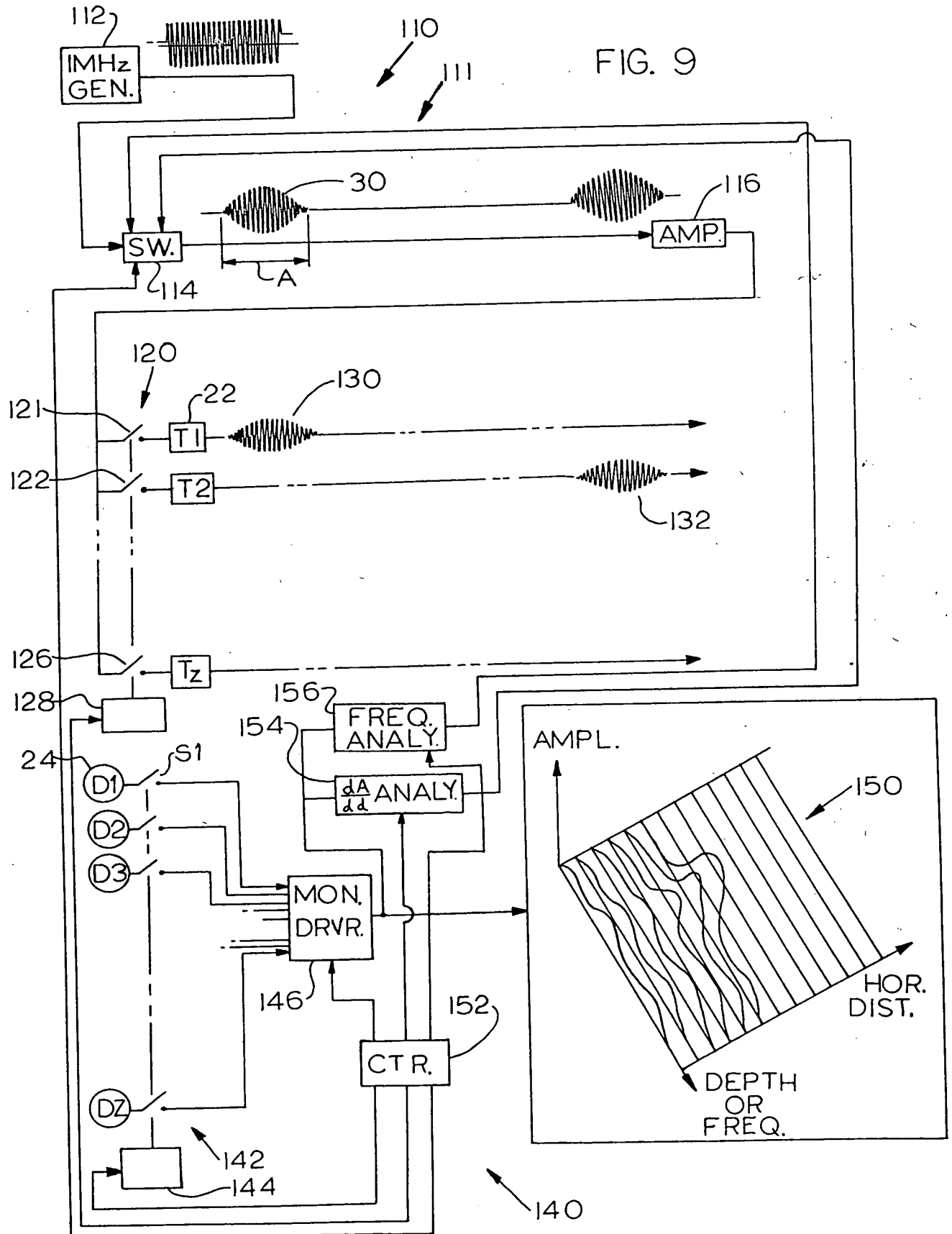


FIG. 10 is a block diagram of a system architecture. The system is divided into two main sections: a ship-based section (174) and a land-based section (176).

Ship-based Section (174): This section includes a ship (174) with a sensor (160) and an antenna (180). The ship is connected to a land-based system (176) via a communication link (182).

Land-based Section (176): This section includes a Central Computer (183), a Display Processing Unit (178), a Fuzzy Expert System, Data Process Algorithms & Fractal Processing, and a Parallel Process Unit. The Central Computer (183) is connected to the Display Processing Unit (178) and the Fuzzy Expert System. The Fuzzy Expert System is connected to the Data Process Algorithms & Fractal Processing, which is in turn connected to the Parallel Process Unit.

Ship's Internal System (182): This section includes an RS-485 interface (162), a Relay (194), a DC Supply (195), a Battery, a PC Cont. (166), a Wave-Form Gen. (164), a DSP Chips (188), a Power Amp (166), and a Prog. Amp. (186). The RS-485 interface (162) is connected to the Relay (194), which is connected to the DC Supply (195). The Battery is connected to the PC Cont. (166). The PC Cont. (166) is connected to the Wave-Form Gen. (164). The Wave-Form Gen. (164) is connected to the DSP Chips (188). The DSP Chips (188) are connected to the Power Amp (166). The Power Amp (166) is connected to the Prog. Amp. (186). The Prog. Amp. (186) is connected to the A/D BD (187).

Land-based System (184): This section includes a Decoder (184), Relays (168), a Pre-Amp (185), and a MUX (172). The Decoder (184) is connected to the Relays (168). The Relays (168) are connected to the Pre-Amp (185). The Pre-Amp (185) is connected to the MUX (172). The MUX (172) is connected to the antenna (180) on the ship.

FIG. 11

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graph LR; MP[MICRO-PROCESSOR CONT.] --> ITH[INTERFACE TO HOST]; MP --> FDB[FIFO DATA BUFFER]; PCC[PROGRAMMABLE CLOCK CONTROLLER] --> FDB; TC[TRIGGER CIRCUIT] --> FDB; FDB --> HSDAC[HIGH SPEED D/A CONVERTER]; HSDAC --> MOD[MODULATOR 192]; SWG[SINE WAVE GENERATOR 190] --> MOD; MOD --> PA[PROGRAMMABLE ATTENUATOR]; PA --> PREA[PRE AMP]; PREA --> POWA[POWER AMP];
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FIG. 12

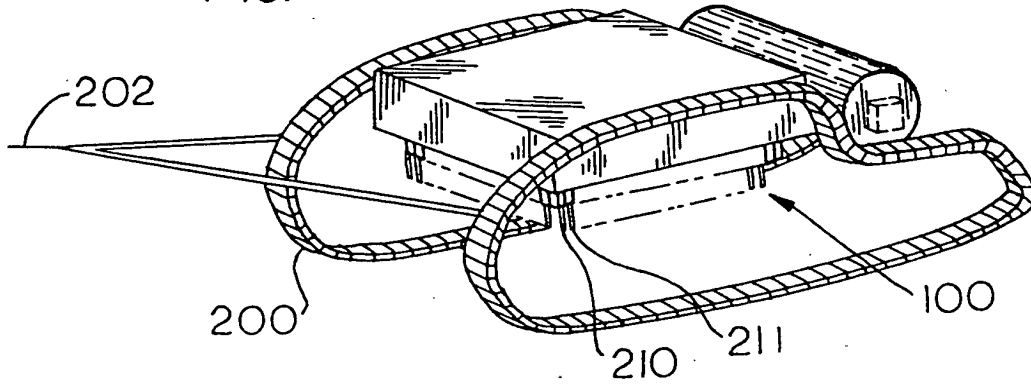
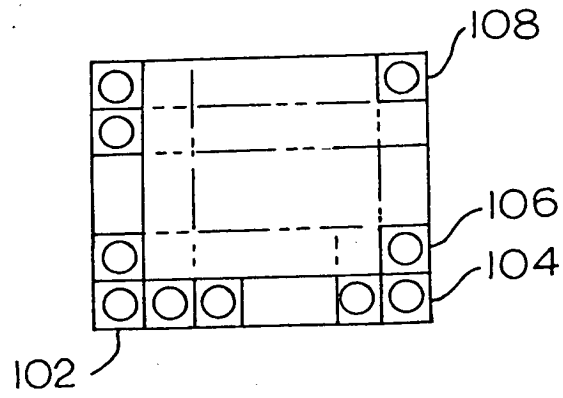


FIG. 12A



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